

Circuit Edit Basics

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Today's leading semiconductor companies use focused ion beam (FIB) tools to perform microsurgery on integrated circuit (IC) devices. Although the use of the FIB for circuit edit (CE) is generally well known within the failure analysis (FA) community, several types of companies could benefit from learning more about its capabilities:

- Companies that are not currently doing any level of CE internally, such as “fabless” design companies. In many cases, these groups already outsource some FIB work to external service labs.
- Companies that already do some level of CE, but may have segments of their design community who are not aware of the FIB's potential for CE.

FIBs are powerful tools for CE because they can remove and deposit materials with high precision. These capabilities can be used to cut and connect circuitry within a device, as well as to create probe points for electrical test. Applications include validating design changes, debugging and optimizing devices in production, and prototyping new devices without costly and time-consuming mask set fabrication.

FIB circuit editing can speed time to market by eliminating iterative cycles of prototype testing and mask modification. FIB-edited device prototypes are used to guide one-time modifications to masks—no more trial and error with successive versions of masks. In addition, FIB prototype devices are often used to enable higher-level testing in order to get a jumpstart on the next round of device modifications.

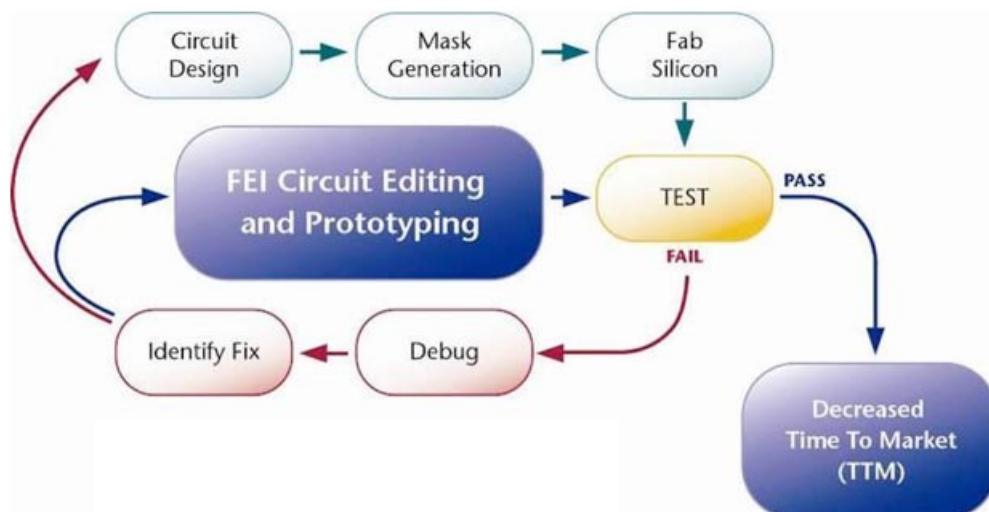


Figure 1 – The value of FIB circuit editing.

Without FIB CE, the development cycle goes like this: After the chip is designed, masks are made, and silicon is fabricated, the part is tested for the first time. Once a problem is found and a fix is determined, it must be validated before becoming part of the final design. This means that the design must be modified and new chips manufactured. This process can take weeks to months to find out whether the fix is correct.

With FIB CE, the fix can be implemented within a day right on the chip and then tested, providing immediate feedback. Several fixes can be collected before committing to new silicon. Finally, prototypes can be made using the fixes, which allows other engineering groups to continue their development work while chips with the new design are still in production.

FIB Basics

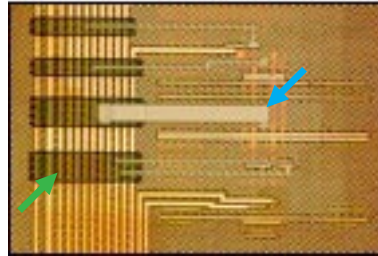
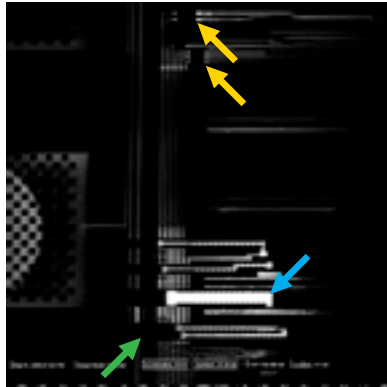
A FIB is very similar to a scanning electron microscope (SEM). A SEM generates a beam of focused electrons, whereas a FIB generates a beam of focused ions (usually Ga^+ ions accelerated to 30–50 KeV). Both generate secondary particles as the primary beam is rastered over the sample surface. These secondary particles are detected and collected to generate a high-resolution image.

Unlike a SEM, however, the ions in the FIB beam have significant mass (and therefore kinetic energy), so the FIB beam can be used to sputter material from the sample surface. Additionally, because two kinds of secondary particles (secondary ions and secondary electrons) are generated when the ion beam strikes the sample surface, a FIB has two possible viewing modes. This is advantageous because some samples are better suited to one mode or the other. For example, secondary electron imaging mode is highly sensitive to whether or not the sample is conductive, whereas secondary ion imaging mode is more sensitive to the surface topography.

During milling, the operator can perform gas-assisted operations by flooding the sample surface with one of various precursor gases. Energy from the ion beam causes adsorbed gas molecules to break down, promoting a localized chemical reaction. If the gas is an etchant like XeF_2 , the etching rate is enhanced. If the gas is a metal-bearing molecule like $\text{W}(\text{CO})_6$, metal lines can be deposited onto the surface. Finally, if the gas is silicon-bearing, insulating materials can be deposited.

An Example of FIB CE Capabilities

The ability to mill away structures and deposit insulating or conducting films makes the FIB a powerful tool for rewiring IC devices.



Figures 2a and 2b – On the left is a FIB view of a sample, and on the right is the corresponding image from a conventional optical microscope.

Figures 2a and 2b illustrate the basic CE tasks a FIB can perform. The yellow arrows mark areas where the FIB beam has been used to cut metal lines. The green arrow indicates a region where insulating films have been deposited. These appear dark in the FIB image and transparent in the optical image. Finally, the blue arrows mark regions where tungsten metal has been deposited. These appear bright in the FIB image and metallic grey in the optical image.

Example of a Simple Frontside Edit

Figure 3 illustrates one of the simplest possible edits.

In this case, the designer asked for a connection between metal layers three and four, and a cut on the metal three line. Overlaid on the FIB image in Figure 3 is the corresponding location from the CAD database. By aligning the CAD image with the visible surface features, we can find buried sub-features.

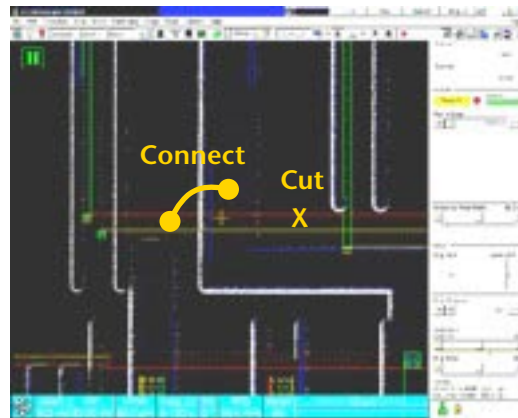


Figure 3 – A simple edit on a four metal-layer part, showing the topography of the top surface metal layer 4 with the CAD overlay.

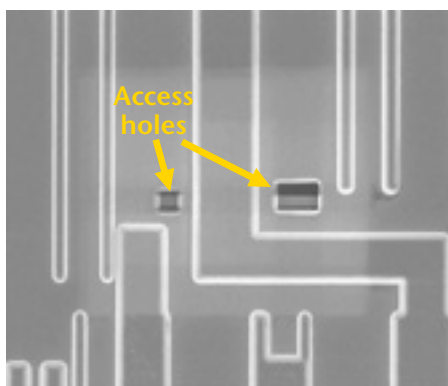


Figure 4 shows two access holes that have been milled to expose the metal three line. The smaller access hole on the left is where the electrical connection will be made, and the larger hole is for cutting the metal line.

Figure 4 – Simple FIB edit in progress.

Figure 5 shows the completed edit. Note the gap in the cut line on the right, and the horizontal strap of FIB-deposited metal on the left.

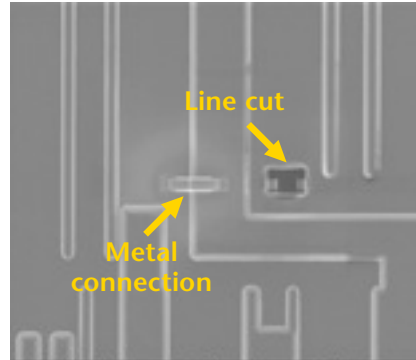


Figure 5 – Simple FIB edit complete.

Figure 6 shows a cross-sectional view of the above edit. The vias labeled a and b were milled to expose metals three and four, respectively. These vias have been filled with FIB-deposited tungsten, and a surface strap of FIB-deposited tungsten joins them (c). On the right is the via that has been milled down to expose and cut the metal three line. That via was also backfilled with FIB-deposited insulating material prior to cross-section.

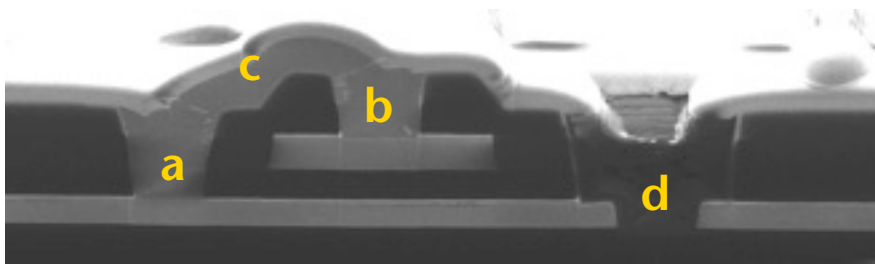
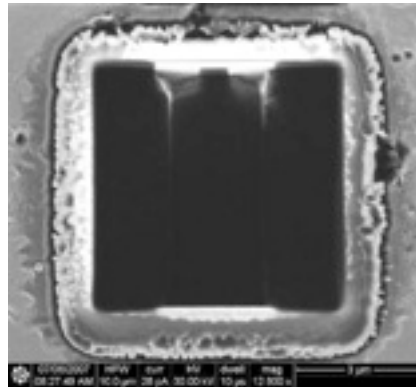
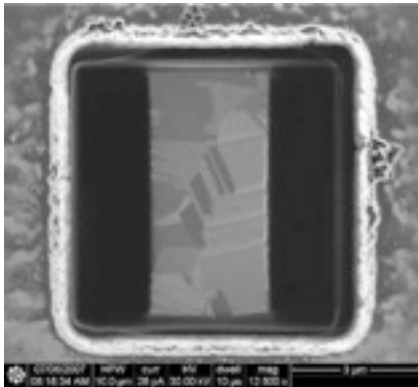


Figure 6 – Cross-section of completed edit.

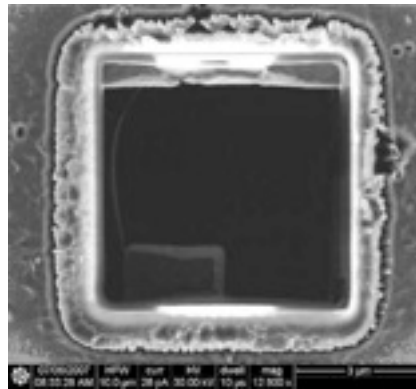
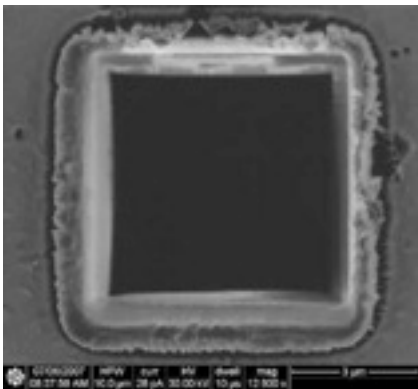
Example of a Complex Frontside Edit

Figures 7–15 illustrate a challenging nine metal-layer frontside edit.

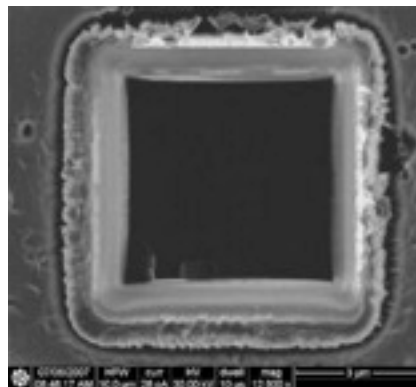
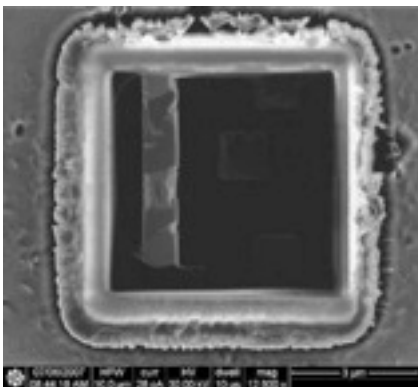
This sequence of 17 images depicts one of the hardest challenges associated with advanced frontside CE: accessing low-lying metal layers. In this case, the task is to drill down through eight layers to expose the metal one layer. It is difficult to cleanly excavate so much material directly over the edit site, because within each layer, the copper and the surrounding dielectric have very different etch rates. Maintaining planarity at each level is a difficult task, one requiring skill and experience.



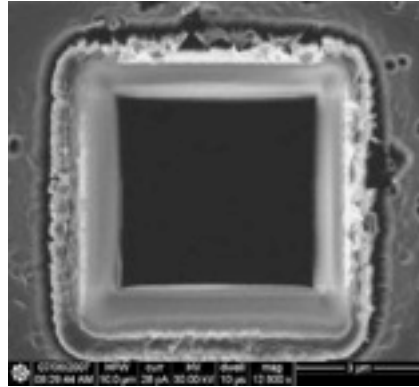
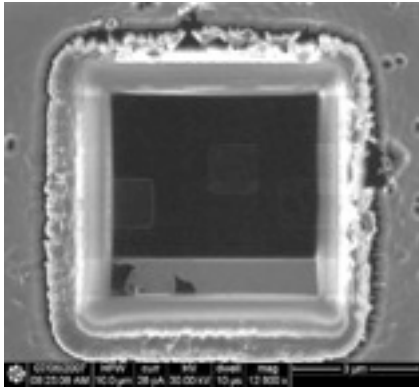
Figures 7a and 7b – Layer nine of complex nine metal-layer edit. Layers are shown both exposed and removed.



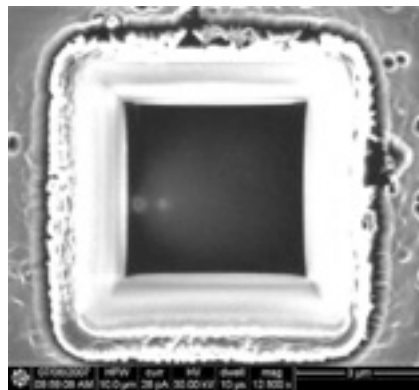
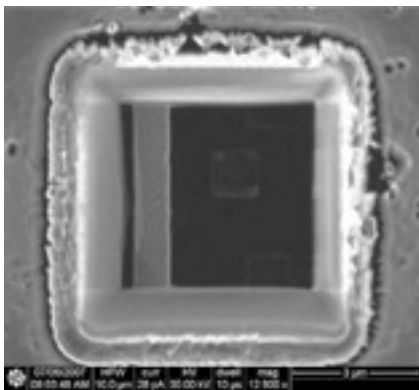
Figures 8a and 8b – Layer eight of complex edit.



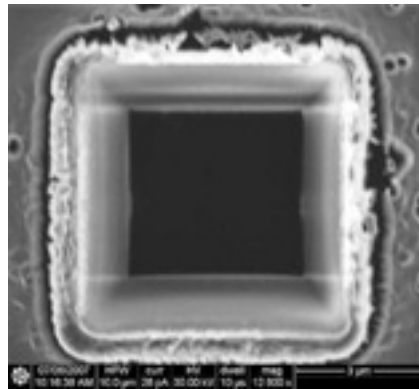
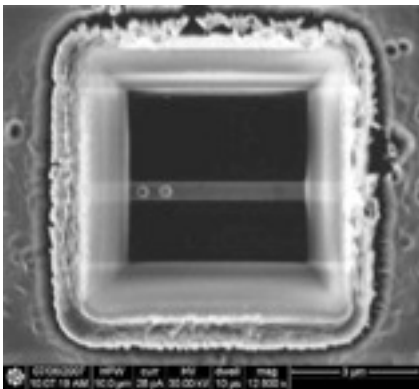
Figures 9a and 9b – Layer seven of complex edit.



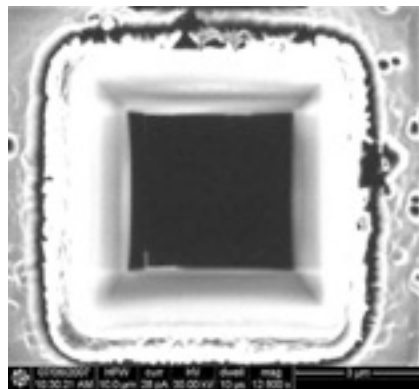
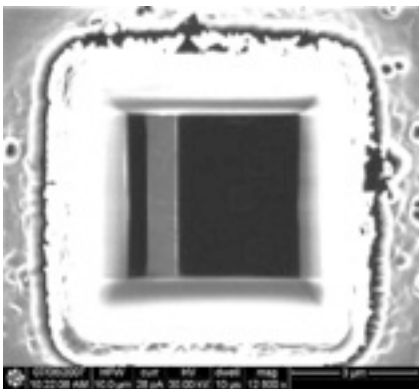
Figures 10a and 10b – Layer six of complex edit.



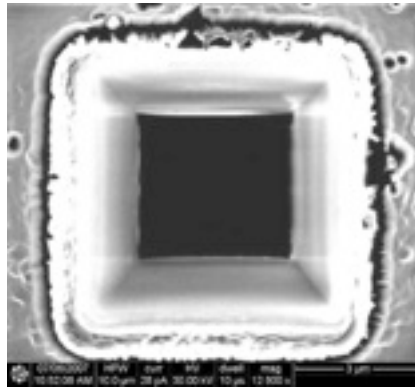
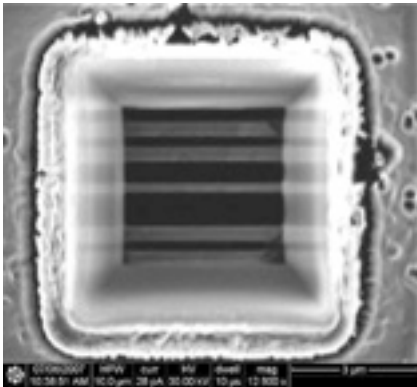
Figures 11a and 11b – Layer five of complex edit.



Figures 12a and 12b – Layer four of complex edit.



Figures 13a and 13b – Layer three of complex edit.



Figures 14a and 14b – Layer two of complex edit.

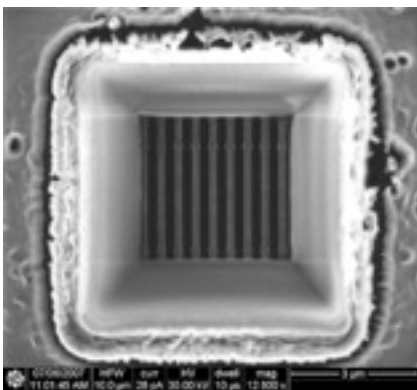


Figure 15 – Layer one of complex edit exposed to metal.

About Backside Editing

Backside editing is becoming increasingly common. Instead of trying to mill through many layers of dense circuitry from the front, operators turn the device over and mill through the substrate silicon to access target areas from the back.

There are three main reasons CE operators may opt for a backside approach. First, access from the frontside may be impractical (as seen above). As IC devices become more complex, the number of layers increases, and the structures become smaller and more tightly packed together. Additionally, IC devices feature an increased abundance of “dummy metals” or “dummy fill,” meaning electrically inactive shapes inserted into the white space of each layer to improve chemical-mechanical planarization (CMP). Copper and dielectric have different milling rates, so as you mill down,

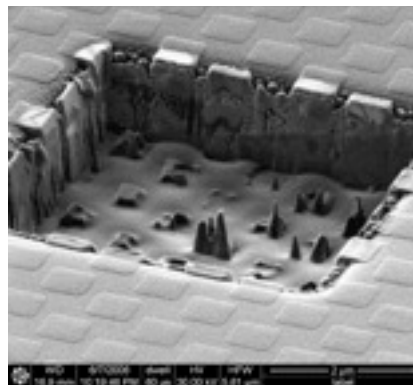
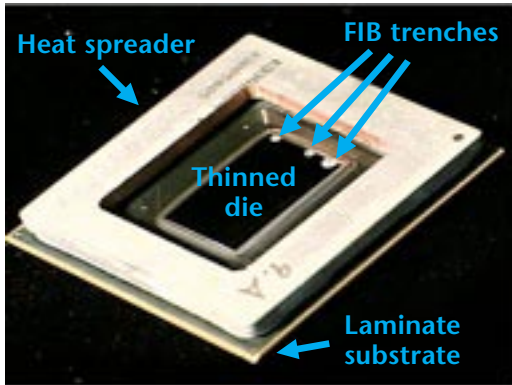


Figure 16 – FIB trench through dummy fill, showing uneven surface at bottom.



topography develops on the trench floor, making it difficult to endpoint on structures of interest.

Figure 17 – Typical BGA-style package, turned over for backside edit.

All of this means that there is less “white space” available to access the target site without killing the device.

Second, new package designs limit access to the frontside of the die.

For example, in ball-grid array (BGA) packages, the front side is completely populated with active solder bumps, which are used to bond the package electrically and mechanically to a motherboard. Any frontside CE activity would result in the destruction of the package.

Finally, backside CE on packaged parts usually allows faster and more convenient iterative electrical testing. Suitable candidates for FIB edit can be thoroughly screened by complete electrical testing more conveniently than with bare die. Additionally, because the mounting surface of the package is not violated, moving between the FIB and the electrical tester for intermediate electrical testing during the edit is straightforward. This is sometimes useful to validate that the electrical characteristics of the device have not changed in unexpected ways during the edit sequence.

Example of a Backside Edit

Figure 17 shows a typical BGA-style package prepared for backside CE. In this case, the central part of the heat spreader has been removed to expose the silicon substrate. Alternatively (and more commonly), the heat spreader can be removed entirely.

After the silicon has been exposed, the substrate is globally thinned using mechanical grinding and polishing techniques, typically to a final silicon thickness of 30–150 micrometers. This limits the time the user has to spend on FIB-milling the substrate silicon to expose the structure of interest.

The silicon is then polished mirror-smooth to ensure optical transparency. The device is then loaded into the FIB, and the operator uses an infrared (IR) microscope to view through the silicon and navigate to the desired target

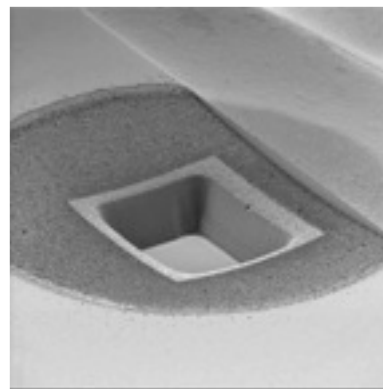


Figure 18 – Magnified FIB trench. Once the overlying substrate silicon has been removed, the operator proceeds to perform the edit.

location. Once the target has been located, the operator begins milling a coarse trench through the silicon. The coarse trench is usually on the order of 50x50 to 200x200 micrometers in size. If the device has multiple edit sites that are more than a few hundred micrometers apart, separate FIB trenches are created for each edit site. Backside FIB trenches are fairly large structures, visible with the naked eye.

Conclusion

The FIB is a versatile and powerful tool, well suited to circuit edit. FIB hardware and techniques are constantly evolving as IC technology evolves, and FIB circuit edits on 45 nanometer devices—while challenging—are possible.sdfsd

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