


*Avago Technologies*

## Copper Milling Enables Thrifty Design-For-Edit ASIC Development

**FEI's CoppeRx™ milling process speeds time-to-market while accelerating understanding of new product performance**

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—David Niles

Failure Analysis Engineer, Avago Technologies

Avago Technologies designs and manufactures analog, mixed-signal, and optoelectronic components and subsystems.

FY2007 net revenue: \$1.5 billion

Headquarters: San Jose, Calif.

[www.avagotech.com](http://www.avagotech.com)

FEI's turnkey CoppeRx process turns an impossible job into an easy and cost-effective way to do circuit edit on ICs with copper layers.

Avago Technologies provides an extensive range of analog, mixed-signal and optoelectronic components and subsystems to manufacturers around the world. With over \$1.5 billion in annual revenue, Avago serves the industrial, automotive, wired networking, wireless communications, and computer peripherals markets. To speed up time-to-market and facilitate understanding of new integrated circuit (IC) performance, the failure analysis engineers at Avago's ASIC Products Division (APD) developed a design-for-edit IC strategy. To aid this process, it was critical to find a way to cut through the circuit's copper metalization quickly and easily. Avago turned to FEI's patented CoppeRx focused ion beam (FIB) copper milling technology to accomplish their goals:

- Find a cost-efficient, uniform method for milling a device's top copper layer
- Leverage production devices as design-for-edit devices, thus avoiding cost-prohibitive mask development for test devices
- Allow a wider group of design engineers to adopt FIB techniques in-house

### The Challenge

Working smartly and efficiently is necessary for profitability in today's semiconductor industry. As a provider of ASIC products featuring copper interconnect, Avago wanted to bring FIB circuit editing in-house to enable a design-for-edit IC strategy. Design-for-edit devices are used only to test the performance parameters of an IC; therefore, they must be made as cost-effectively as possible. “Acquiring this capability in-house is critical for fast turn-around of test results at a reasonable cost. The time and expense of external vendors creates a hurdle that discourages design teams from using FIBs to solve problems and promote learning,” says David Niles, a failure analysis engineer with Avago Technologies, ASIC Product Division, Fort Collins, Colo. “Prior to the development of CoppeRx, FIB milling was unsuitable for copper because it milled unevenly, creating a mess and potentially destroying the device,” says Niles.

**Why FEI**

According to Dr. Niles, “Working with FEI is very satisfying. They have an expert staff and are very attentive to Avago’s needs. FEI developed CoppeRx so I didn’t have to reinvent the wheel. I called to ask for the applications engineer’s advice. He recommended CoppeRx. He said I could use it right out of the box—and I did. I used it straight out of the box and it worked. Working with FEI has enabled me to perform difficult edits down to 45nm. I am really successful in the copper arena because of FEI’s help.”

**The Solution**

FEI’s CoppeRx FIB copper milling process for advanced circuit edit, combined with gas chemistry, delivers uniform milling rates regardless of how the copper interconnect is produced. Avago purchased an FEI FIB equipped with the CoppeRx process for circuit editing at the 90nm, 65nm and 45nm technology nodes. “Cutting copper bus lines without the CoppeRx process is extremely difficult because some copper grains are nearly impervious to the beam. CoppeRx made it a turn-key operation, facilitating the circuit edit,” says Niles.

**The Result**

The FIB’s advanced copper milling process allows Avago design engineers to develop creative design-for-edit circuits to shorten the learning cycle. “Today copper milling is a task that can be done quickly with a 100 percent success rate. Plus, we can use a single chip for multiple purposes to save thousands of dollars per year,” notes Niles.

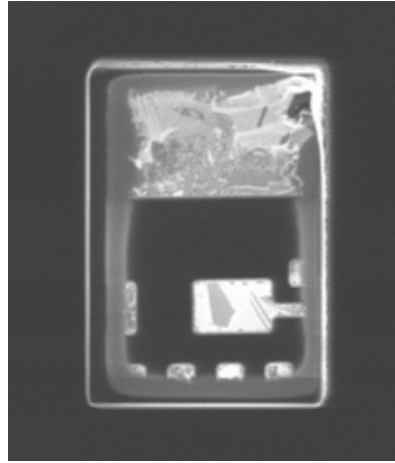


Fig. 1a: The top-layer copper bus line on a flip chip part before packaging. A small cut has been made through the passivation to expose the top layer copper bus and an adjacent, unattached node.

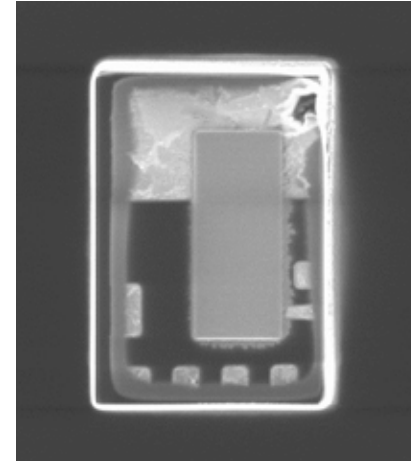


Fig. 1b: A tungsten jumper drawn in the VectraVision FIB connects the node to the grounded copper bus line.



Fig. 2a: A second opening exposes the copper bus line between the jumper and the ground source. The jumper, further down the bus line, is not in the field of view.

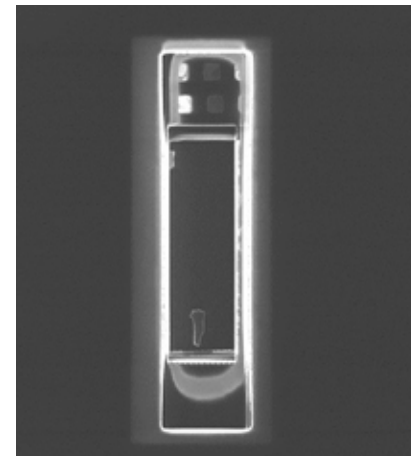


Fig. 2b: The CoppeRx process cleanly cuts the copper bus line, releasing the bump and jumpered node from ground. The design-for-edit fix is now complete, with the node connected to the solder bump and free from ground.

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